ADuM160N/ADuM161N/ADuM162N/ADuM163N

3.0 kV RMS, 6-Channel Digital Isolators

FEATURES

- High common-mode transient immunity: 100 kV/µs
- High robustness to radiated and conducted noise
- Low propagation delay
  - 13 ns maximum for 5 V operation
  - 15 ns maximum for 1.8 V operation
- 150 Mbps maximum guaranteed data rate
- Safety and regulatory approvals (pending)
  - UL 1577
    - V_{ISO} = 3000 V rms for 1 minute
  - IEC/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB 4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 565 V peak
- Low dynamic power consumption
- 1.8 V to 5 V level translation
- High temperature operation: 125°C
- Fail-safe high or low options
- 16-lead, RoHS-compliant, narrow-body SOIC package

APPLICATIONS

- General-purpose multichannel isolation
- Serial peripheral interface (SPI)/data converter isolation
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM160N/ADuM161N/ADuM162N/ADuM163N[1] are 6-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 4.5 ns at 5 V operation. Channel to channel matching of propagation delay is tight at 4.0 ns maximum.

The ADuM160N/ADuM161N/ADuM162N/ADuM163N data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3.0 kV rms (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 1.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available by which the outputs transition to a predetermined state when the input power supply is not applied.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. B

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REVISION HISTORY

2/2025—Rev. A to Rev. B

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FUNCTIONAL BLOCK DIAGRAMS

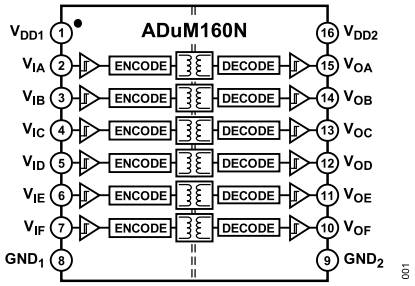

Figure 1. ADuM160N Functional Block Diagram

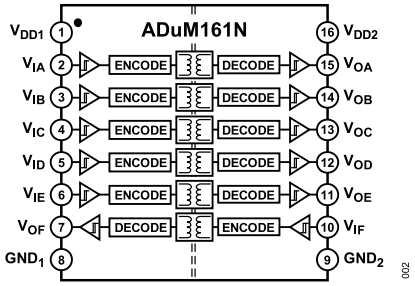

Figure 2. ADuM161N Functional Block Diagram

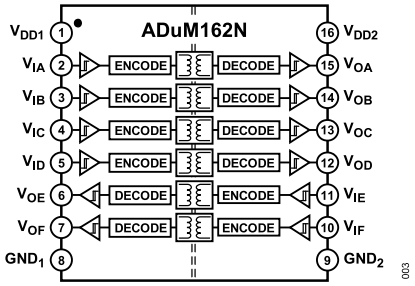

Figure 3. ADuM162N Functional Block Diagram

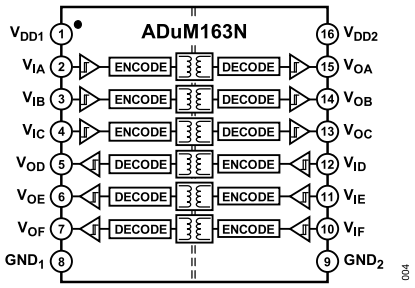

Figure 4. ADuM163N Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	4.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	4.0	ns	
Opposing Direction	t_{PSKOD}		0.5	4.5	ns	
Jitter			490		ps p-p	See the Jitter Measurement section
			70		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −4 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM160N						
	$I_{DD1 (Q)}$		2.3	3.5	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.3	4.52	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		19.3	30	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		3.5	4.82	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM161N						
	$I_{DD1 (Q)}$		2.5	3.8	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.2	4.22	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		16.0	24.8	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		7.2	11.2	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM162N						
	$I_{DD1 (Q)}$		2.8	4.0	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.0	4.2	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		14.1	22.5	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		10.5	16.7	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM163N						
	$I_{DD1 (Q)}$		3.0	4.26	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.8	3.92	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		11.8	18.9	mA	V_I[5] = 1 (N0), 0 (N1)[6]

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		14.6	23	mA	V_I[5] = 1 (N0), 0 (N1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\lvert CM_H \rvert$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[3] V_{IxH} is the input side logic high.

[4] V_{IxL} is the input side logic low.

[5] V_I is the voltage input.

[6] N0 refers to the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 models. N1 refers to the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 models. See the Ordering Guide section.

[7] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM160N											
Supply Current Side 1	I_{DD1}		10.8	15.8		12.3	19.2		18.3	26	mA
Supply Current Side 2	I_{DD2}		3.6	5.5		5.63	9.0		12.8	20.9	mA
ADuM161N											
Supply Current Side 1	I_{DD1}		9.27	14.5		10.9	17.2		17.3	25.6	mA
Supply Current Side 2	I_{DD2}		5.33	9.0		7.39	12		14.5	22.2	mA
ADuM162N											
Supply Current Side 1	I_{DD1}		8.53	13.0		10.2	15.6		16.4	25.5	mA
Supply Current Side 2	I_{DD2}		6.83	10.5		8.64	13.1		14.6	22.3	mA
ADuM163N											
Supply Current Side 1	I_{DD1}		7.47	12.3		9.35	14.5		15.9	23	mA
Supply Current Side 2	I_{DD2}		8.75	14.0		10.5	16.0		17.0	23.3	mA

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	4.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	4.0	ns	
Opposing Direction	t_{PSKOD}		0.7	4.5	ns	
Jitter			580		ps p-p	See the Jitter Measurement section
			120		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM160N						
	$I_{DD1 (Q)}$		2.2	3.4	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.1	4.1	mA	V_I[5] = 0 (N0), 1 (N1)[66]
	$I_{DD1 (Q)}$		19	27.7	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		3.4	4.7	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM161N						
	$I_{DD1 (Q)}$		2.3	3.6	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.0	4.0	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		15.8	24.6	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		7.0	11	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM162N						
	$I_{DD1 (Q)}$		2.6	3.8	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.8	4.0	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		13.9	22.2	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		10.3	16.5	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM163N						
	$I_{DD1 (Q)}$		2.8	4.16	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.6	3.82	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		11.5	18.5	mA	V_I[5] = 1 (N0), 0 (N1)[6]

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		14.3	22.5	mA	V_I[5] = 1 (N0), 0 (N1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[3] V_{IxH} is the input side logic high.

[4] V_{IxL} is the input side logic low.

[5] V_I is the voltage input.

[6] N0 refers to the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 models. N1 refers to the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 models. See the Ordering Guide section.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM160N											
Supply Current Side 1	I_{DD1}		10.5	15.5		11.7	18.6		16.6	24.6	mA
Supply Current Side 2	I_{DD2}		3.4	5.4		5.4	7.8		11.8	19.9	mA
ADuM161N											
Supply Current Side 1	I_{DD1}		9.0	14.2		10.4	16.6		15.7	24.1	mA
Supply Current Side 2	I_{DD2}		5.1	8.8		7.0	11.6		13.1	20.8	mA
ADuM162N											
Supply Current Side 1	I_{DD1}		8.3	12.8		9.8	14.8		15.2	24.3	mA
Supply Current Side 2	I_{DD2}		6.6	10.3		8.3	12.6		13.8	21.5	mA
ADuM163N											
Supply Current Side 1	I_{DD1}		7.3	12		8.9	14.2		14.9	22	mA
Supply Current Side 2	I_{DD2}		8.5	13.7		9.9	15.6		16	22.3	mA

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two units at the same temperature, voltage, load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	5.0	ns	
Opposing Direction	t_{PSKOD}		0.7	5.0	ns	
Jitter			800		ps p-p	See the Jitter Measurement section
			190		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM160N						
	$I_{DD1 (Q)}$		2.1	3.3	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.1	4.1	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		19	27.7	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		3.3	4.6	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM161N						
	$I_{DD1 (Q)}$		2.2	3.5	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.9	3.9	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		15.7	24.5	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		6.9	10.9	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM162N						
	$I_{DD1 (Q)}$		2.5	3.7	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.7	3.9	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		13.8	22.1	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		10.2	16.4	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM163N						
	$I_{DD1 (Q)}$		2.7	4.08	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.55	3.72	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		11.5	18.4	mA	V_I[5] = 1 (N0), 0 (N1)[6]

SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		14.3	22.3	mA	V_I[5] = 1 (N0), 0 (N1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\lvert CM_H \rvert$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[3] V_{IxH} is the input side logic high.

[4] V_{IxL} is the input side logic low.

[5] V_I is the voltage input.

[6] N0 refers to the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 models. N1 refers to the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 models. See the Ordering Guide section.

[7] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 VDDx. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM160N											
Supply Current Side 1	I_{DD1}		10.4	15.4		11.2	18.4		16	24	mA
Supply Current Side 2	I_{DD2}		3.3	5.3		4.8	7.2		9.8	17.9	mA
ADuM161N											
Supply Current Side 1	I_{DD1}		8.9	14.1		10.1	16.3		14.8	23.6	mA
Supply Current Side 2	I_{DD2}		5.0	8.7		6.5	11.1		11.4	20.1	mA
ADuM162N											
Supply Current Side 1	I_{DD1}		8.1	12.6		9.4	14.4		14.1	23.2	mA
Supply Current Side 2	I_{DD2}		6.5	10.2		7.8	12.1		12.4	20.1	mA
ADuM163N											
Supply Current Side 1	I_{DD1}		7.1	11.9		8.5	13.9		13.6	21	mA
Supply Current Side 2	I_{DD2}		8.3	13.4		9.7	15.2		14.8	21.3	mA

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 1.8 V. Minimum/maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	5.0	ns	
Opposing Direction	t_{PSKOD}		0.7	5.0	ns	
Jitter			470		ps p-p	See the Jitter Measurement section
			70		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
ADuM160N						
	$I_{DD1 (Q)}$		2.0	3.2	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		3.0	4.0	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		18.7	27.4	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		3.3	4.6	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM161N						
	$I_{DD1 (Q)}$		2.1	3.4	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.9	3.9	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		15.5	24.3	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		6.8	10.8	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM162N						
	$I_{DD1 (Q)}$		2.4	3.6	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.7	3.9	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		13.7	22	mA	V_I[5] = 1 (N0), 0 (N1)[6]
	$I_{DD2 (Q)}$		10.1	16.3	mA	V_I[5] = 1 (N0), 0 (N1)[6]
ADuM163N						
	$I_{DD1 (Q)}$		2.6	4.03	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD2 (Q)}$		2.5	3.72	mA	V_I[5] = 0 (N0), 1 (N1)[6]
	$I_{DD1 (Q)}$		11.3	18.3	mA	V_I[5] = 1 (N0), 0 (N1)[6]

SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2 (Q)}$		14	22	mA	V_I[5] = 1 (N0), 0 (N1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, D, E, or F.

[3] V_{IxH} is the input side logic high.

[4] VIxL is the input side logic low.

[5] V_I is the voltage input.

[6] N0 refers to the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 models. N1 refers to the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 models. See the Ordering Guide section.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM160N											
Supply Current Side 1	I_{DD1}		10.2	15.2		11.3	18.2		15.9	23.9	mA
Supply Current Side 2	I_{DD2}		3.3	5.3		4.8	7.2		9.8	17.9	mA
ADuM161N											
Supply Current Side 1	I_{DD1}		8.7	13.9		10	16.2		14.6	23.4	mA
Supply Current Side 2	I_{DD2}		4.9	8.6		6.4	11		11.4	20.1	mA
ADuM162N											
Supply Current Side 1	I_{DD1}		8.0	12.5		9.2	14.2		13.9	23	mA
Supply Current Side 2	I_{DD2}		6.4	10.1		7.7	12		12.4	20.1	mA
ADuM163N											
Supply Current Side 1	I_{DD1}		7.0	11.8		8.3	13.7		13.3	20.7	mA
Supply Current Side 2	I_{DD2}		8.2	13.3		9.5	15		14.5	21	mA

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see http://www.analog.com/icouplersafety.

Table 9.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0[1, 2]	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

1 In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 meters.

2 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

PACKAGE CHARACTERISTICS

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		75		°C/W	Thermocouple located at center of package underside

1 The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

2 Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM160N/ADuM161N/ADuM162N/ADuM163N certification approvals are listed in Table 11.

Table 11.

UL	CSA	VDE	CQC
UL 1577[1]	IEC/CSA 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)[2]	CQC GB 4943.1
Single Protection, 3000 V rms	Basic insulation, 400 V rms	Reinforced insulation, 565 V peak	Basic insulation, 400 V rms
	Reinforced insulation, 200 V rms		
	IEC/CSA 60601-1		
	Basic insulation (1 MOPP), 250 V rms		
	IEC/CSA 61010-1		
	Basic insulation, 300 V rms, Overvoltage Category III		
	Reinforced insulation, 150 V rms		
File E214100	File No. 205078	Certificate No. 40051926	Certificate No. CQC18001196412

1 In accordance with UL 1577, each ADuM160N/ADuM161N/ADuM162N/ADuM163N in the R-16, narrow-body (SOIC_N) package is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

SPECIFICATIONS

[2] In accordance with DIN EN IEC 60747 (VDE 0884-17) each ADuM160N/ADuM161N/ADuM162N/ADuM163N in the R-16, narrow-body (SOIC_N) package is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 12.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
≤ 150 V rms			I to IV	
≤ 300 V rms			I to IV	
≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	565	V peak
Maximum Working Insulation Voltage		V_{IOWM}	400	V rms
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1059	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	904	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	678	V peak
Maximum Transient Isolation Voltage	V_{TEST} = 1.2 × V_{IOTM}, t = 1 sec (100% production)	V_{IOTM}	4200	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	4200	V peak
Maximum Surge Isolation Voltage	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 5)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.64	W
Insulation Resistance at T_S		R_S	$>10^9$	Ω

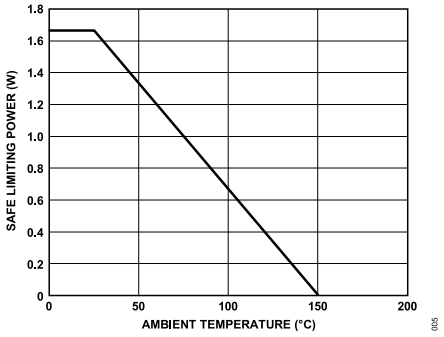

Figure 5. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 13.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages	V_{DD1}, V_{DD2}	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 14.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE}, V_{IF})	−0.5 V to V_{DDI}[1] + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD}, V_{OE}, V_{OF})	−0.5 V to V_{DDO}[2] + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/µs to +150 kV/µs

[1] V_{DDI} is the input side supply voltage.

[2] V_{DDO} is the output side supply voltage.

[3] See Figure 5 for the maximum rated current values for various temperatures.

[4] Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 15. Maximum Continuous Working Voltage[1]

Parameter	Rating	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	565	V peak	Reinforced insulation rating per IEC 60747-17 (VDE 0884-17)

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ABSOLUTE MAXIMUM RATINGS

TRUTH TABLE

Table 16. ADuM160N/ADuM161N/ADuM162N/ADuM163N Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (N0), V_{Ox} Output[1, 2, 3]	Default High (N1), V_{Ox} Output[1, 2, 3]	Test Conditions/Comments
L	Powered	Powered	L	L	Normal operation
H	Powered	Powered	H	H	Normal operation
L	Unpowered	Powered	L	H	Fail-safe output
X[4]	Powered	Unpowered	Indeterminate	Indeterminate	Output Unpowered

[1] L means low, H means high, and X means don't care.

[2] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, D, E or F). V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

[3] N0 refers to the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 models. N1 refers to the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 models. See the Ordering Guide section.

[4] Input pins (V_{Ix}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

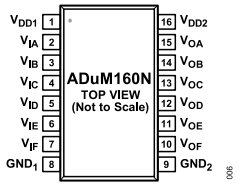

Figure 6. ADuM160N Pin Configuration

Table 17. ADuM160N Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{IE}	Logic Input E.
7	V_{IF}	Logic Input F.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{OF}	Logic Output F.
11	V_{OE}	Logic Output E.
12	V_{OD}	Logic Output D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

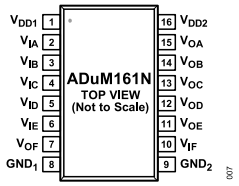

Figure 7. ADuM161N Pin Configuration

Table 18. ADuM161N Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{IE}	Logic Input E.
7	V_{OF}	Logic Output F.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{IF}	Logic Input F.
11	V_{OE}	Logic Output E.
12	V_{OD}	Logic Output D.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 18. ADuM161N Pin Function Descriptions (Continued)

Pin No.[1]	Mnemonic	Description
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

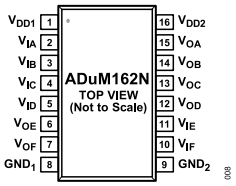

Figure 8. ADuM162N Pin Configuration

Table 19. ADuM162N Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{OE}	Logic Output E.
7	V_{OF}	Logic Output F.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{IF}	Logic Input F.
11	V_{IE}	Logic Input E.
12	V_{OD}	Logic Output D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

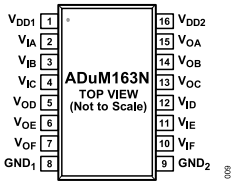

Figure 9. ADuM163N Pin Configuration

Table 20. ADuM163N Pin Function Descriptions

Pin No.[1]	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 20. ADuM163N Pin Function Descriptions (Continued)

Pin No.[1]	Mnemonic	Description
4	V_{IC}	Logic Input C.
5	V_{OD}	Logic Output D.
6	V_{OE}	Logic Output E.
7	V_{OF}	Logic Output F.
8	GND_1	Ground 1. Ground reference for Isolator Side 1.
9	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{IF}	Logic Input F.
11	V_{IE}	Logic Input E.
12	V_{ID}	Logic Input D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

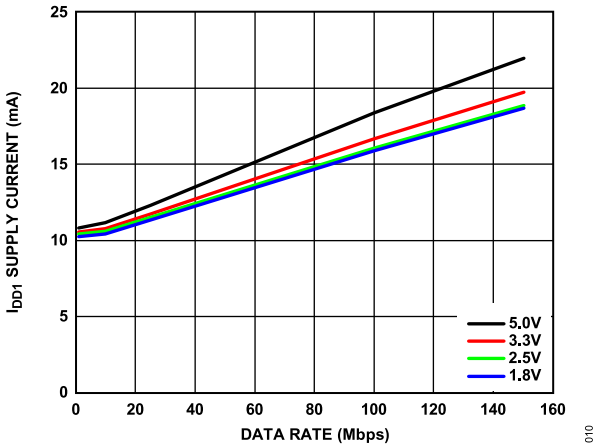

Figure 10. ADuM160N I_{DD1} Supply Current vs. Data Rate at Various Voltages

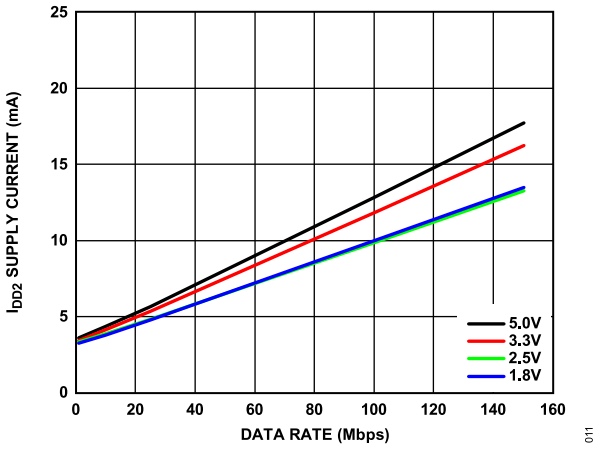

Figure 11. ADuM160N I_{DD2} Supply Current vs. Data Rate at Various Voltages

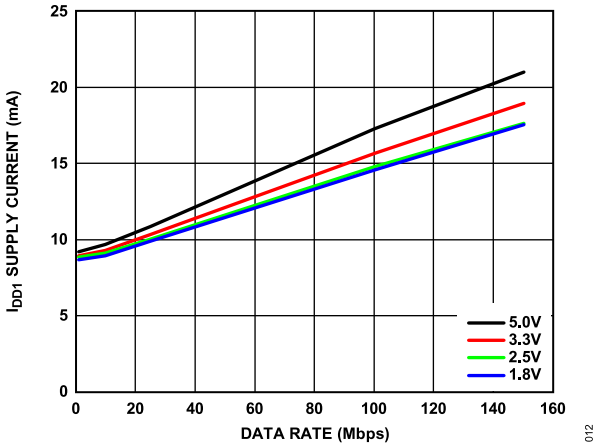

Figure 12. ADuM161N I_{DD1} Supply Current vs. Data Rate at Various Voltages

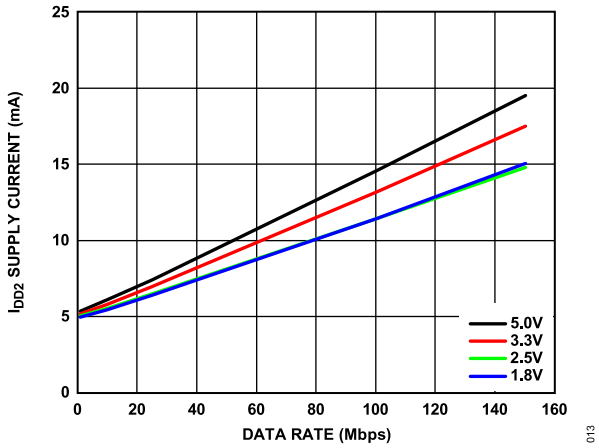

Figure 13. ADuM161N I_{DD2} Supply Current vs. Data Rate at Various Voltages

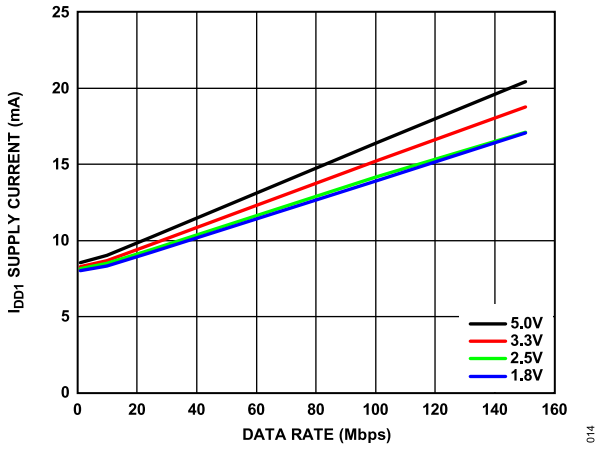

Figure 14. ADuM162N I_{DD1} Supply Current vs. Data Rate at Various Voltages

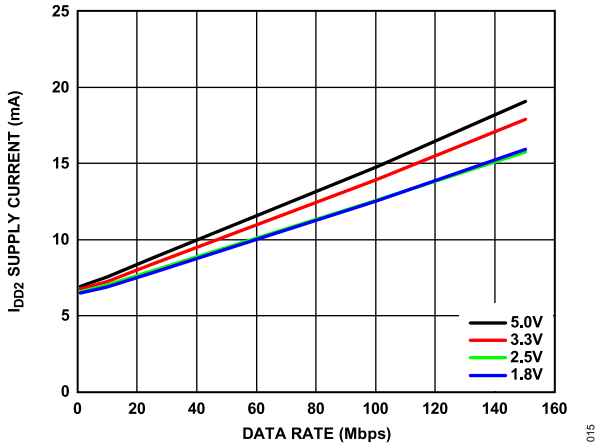

Figure 15. ADuM162N I_{DD2} Supply Current vs. Data Rate at Various Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

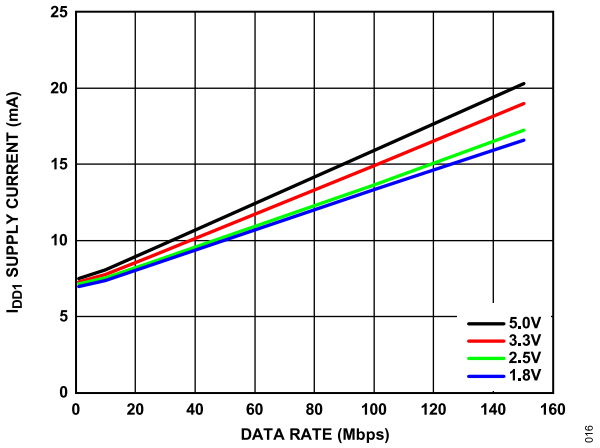

Figure 16. ADuM163N I_{DD1} Supply Current vs. Data Rate at Various Voltages

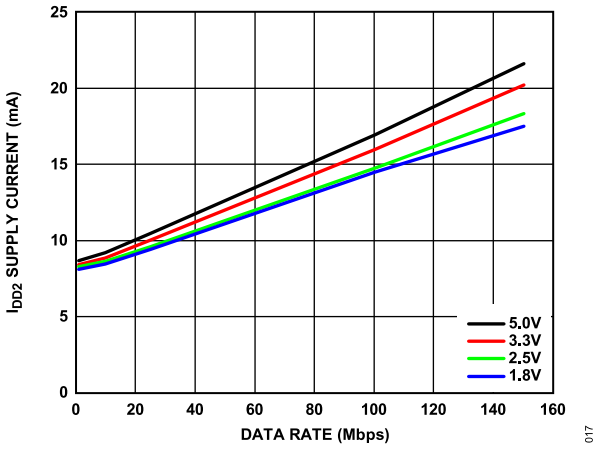

Figure 17. ADuM163N I_{DD2} Supply Current vs. Data Rate at Various Voltages

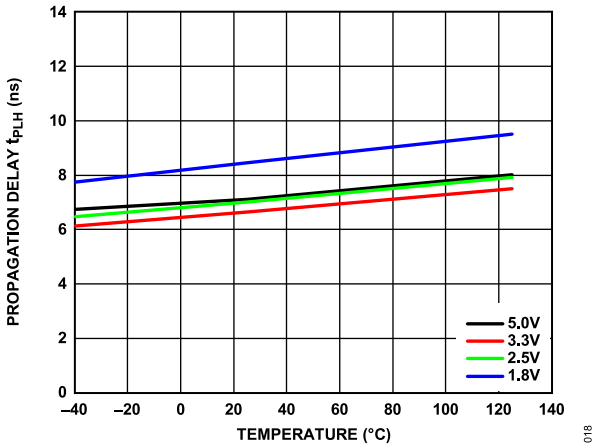

Figure 18. Propagation Delay, t_{PLH} vs. Temperature at Various Voltages

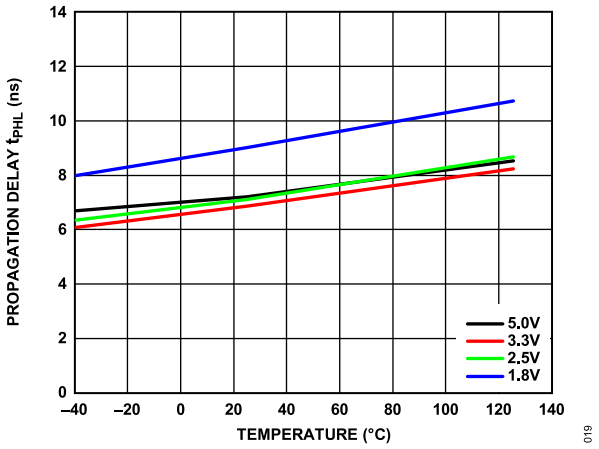

Figure 19. Propagation Delay, t_{PHL} vs. Temperature at Various Voltages

THEORY OF OPERATION

The ADuM160N/ADuM161N/ADuM162N/ADuM163N use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 20 and Figure 21, the ADuM160N/ADuM161N/ADuM162N/ADuM163N have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 20 shows the waveforms for models of the ADuM160N0/ADuM161N0/ADuM162N0/ADuM163N0 that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the fail-safe output state of low sets the output to low. For the ADuM160N1/ADuM161N1/ADuM162N1/ADuM163N1 that have a fail-safe output state of high, Figure 21 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

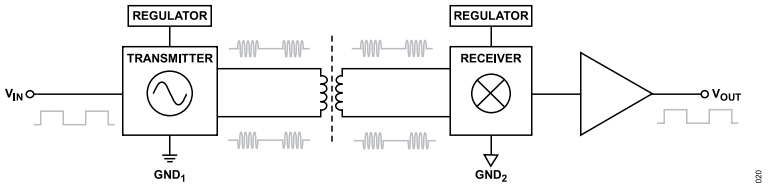

Figure 20. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

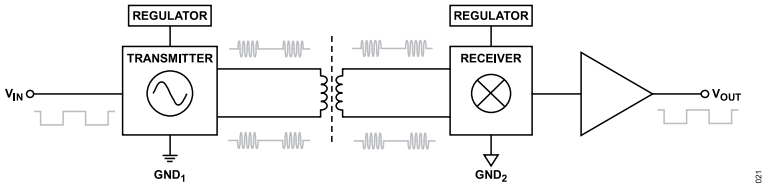

Figure 21. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM160N/ADuM161N/ADuM162N/ADuM163N digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 22). Bypass capacitors are connected between Pin 1 and Pin 8 for V_{DD1} and between Pin 9 and Pin 16 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

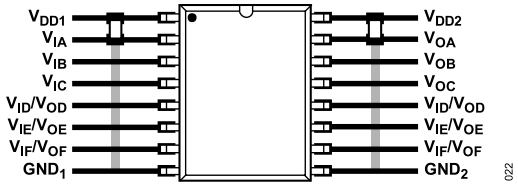

Figure 22. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

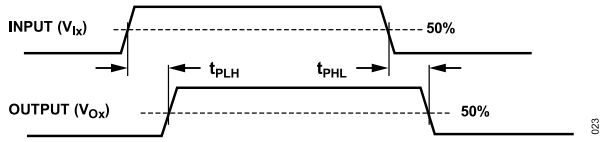

Figure 23. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM160N/ADuM161N/ADuM162N/ADuM163N component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple ADuM160N/ADuM161N/ADuM162N/ADuM163N components operating under the same conditions.

JITTER MEASUREMENT

Figure 24 illustrates the eye diagram for the ADuM160N/ADuM161N/ADuM162N/ADuM163N. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS) 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM160N/ADuM161N/ADuM162N/ADuM163N with 490 ps p-p jitter.

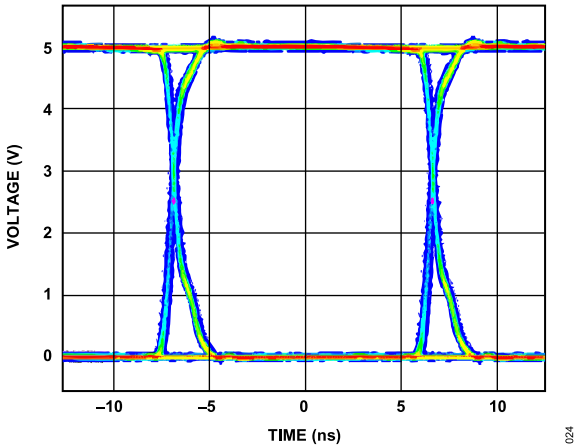

Figure 24. ADuM160N/ADuM161N/ADuM162N/ADuM163N Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM160N/ADuM161N/ADuM162N/ADuM163N.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 15 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-16	SOIC_N	16-Lead Standard Small Outline Package, Narrow Body

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM160N1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM160N1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM160N0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM160N0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM161N1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM161N1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM161N0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM161N0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM162N1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM162N1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM162N0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM162N0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM163N1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM163N1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16
ADuM163N0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM163N0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N, 7” Reel	Reel, 1000	R-16

[1] Z = RoHS Compliant Part.

NUMBER OF INPUTS (V_{DD1} SIDE AND V_{DD2} SIDE), WITHSTAND VOLTAGE RATING, AND FAIL-SAFE OUTPUT STATE OPTIONS

Model[1]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State
ADuM160N1BRZ	6	0	3.0	High
ADuM160N1BRZ-RL7	6	0	3.0	High
ADuM160N0BRZ	6	0	3.0	Low
ADuM160N0BRZ-RL7	6	0	3.0	Low
ADuM161N1BRZ	5	1	3.0	High
ADuM161N1BRZ-RL7	5	1	3.0	High
ADuM161N0BRZ	5	1	3.0	Low
ADuM161N0BRZ-RL7	5	1	3.0	Low
ADuM162N1BRZ	4	2	3.0	High
ADuM162N1BRZ-RL7	4	2	3.0	High
ADuM162N0BRZ	4	2	3.0	Low
ADuM162N0BRZ-RL7	4	2	3.0	Low
ADuM163N1BRZ	3	3	3.0	High
ADuM163N1BRZ-RL7	3	3	3.0	High
ADuM163N0BRZ	3	3	3.0	Low
ADuM163N0BRZ-RL7	3	3	3.0	Low

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
EVAL-5CH6CHSOICEBZ	Unpopulated Evaluation Board
EVAL-ADuM163N0EBZ	Populated Evaluation Board

[1] Z = RoHS Compliant Part.